

FIG. 1a

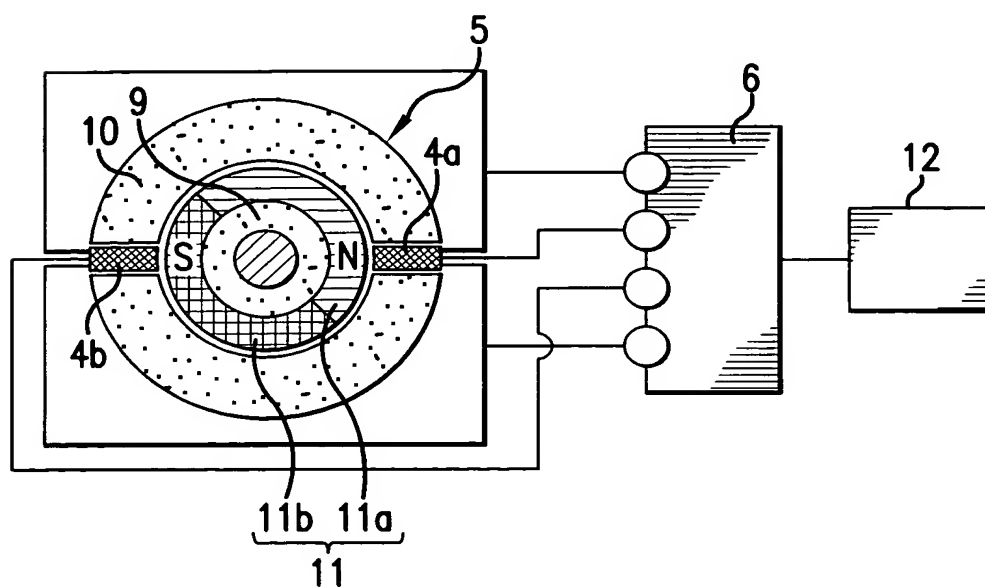


FIG. 1b

#D~VOLTAGE STUCK FAILURE OF THE SECOND IC 4b IS GENERATED

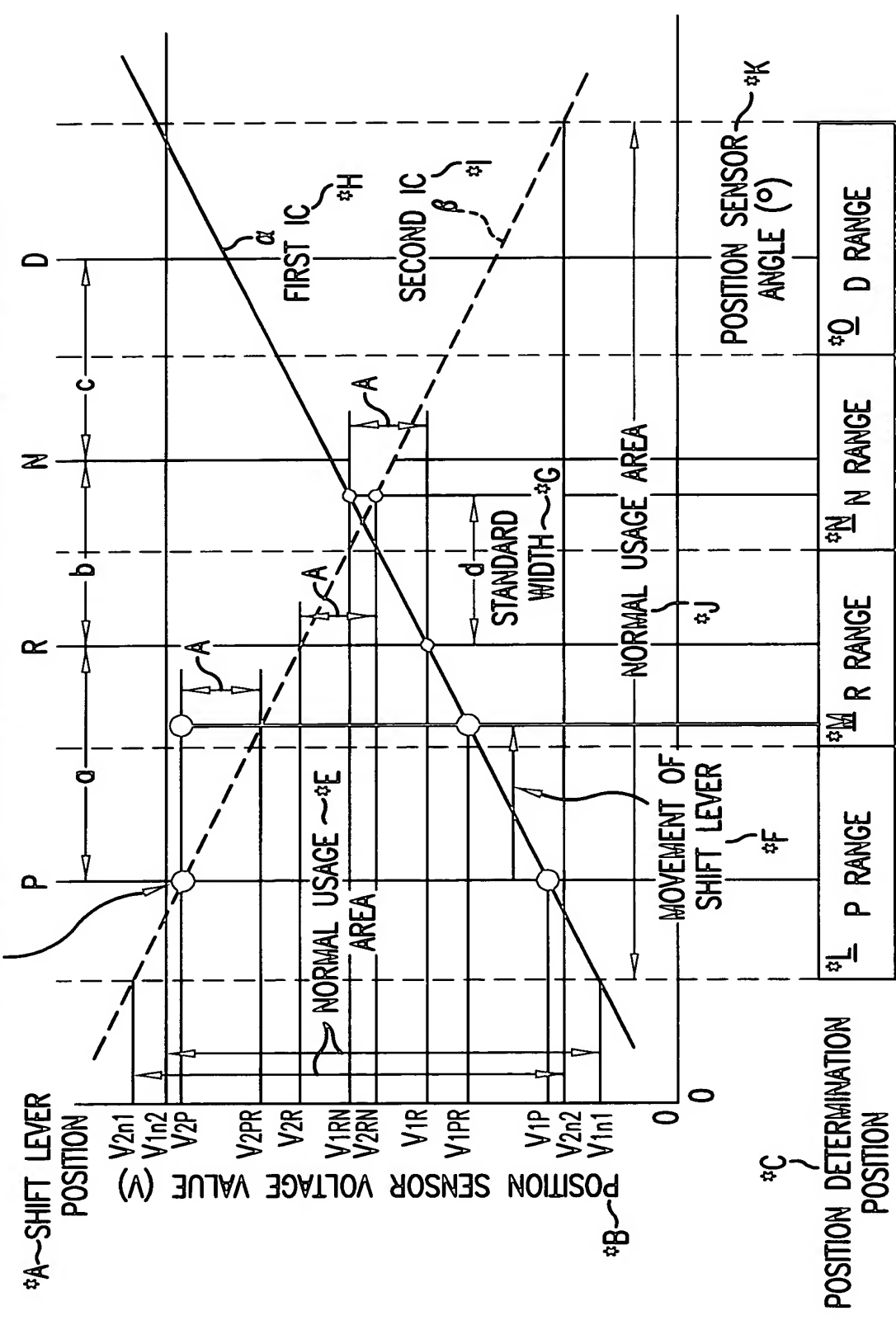


FIG.2

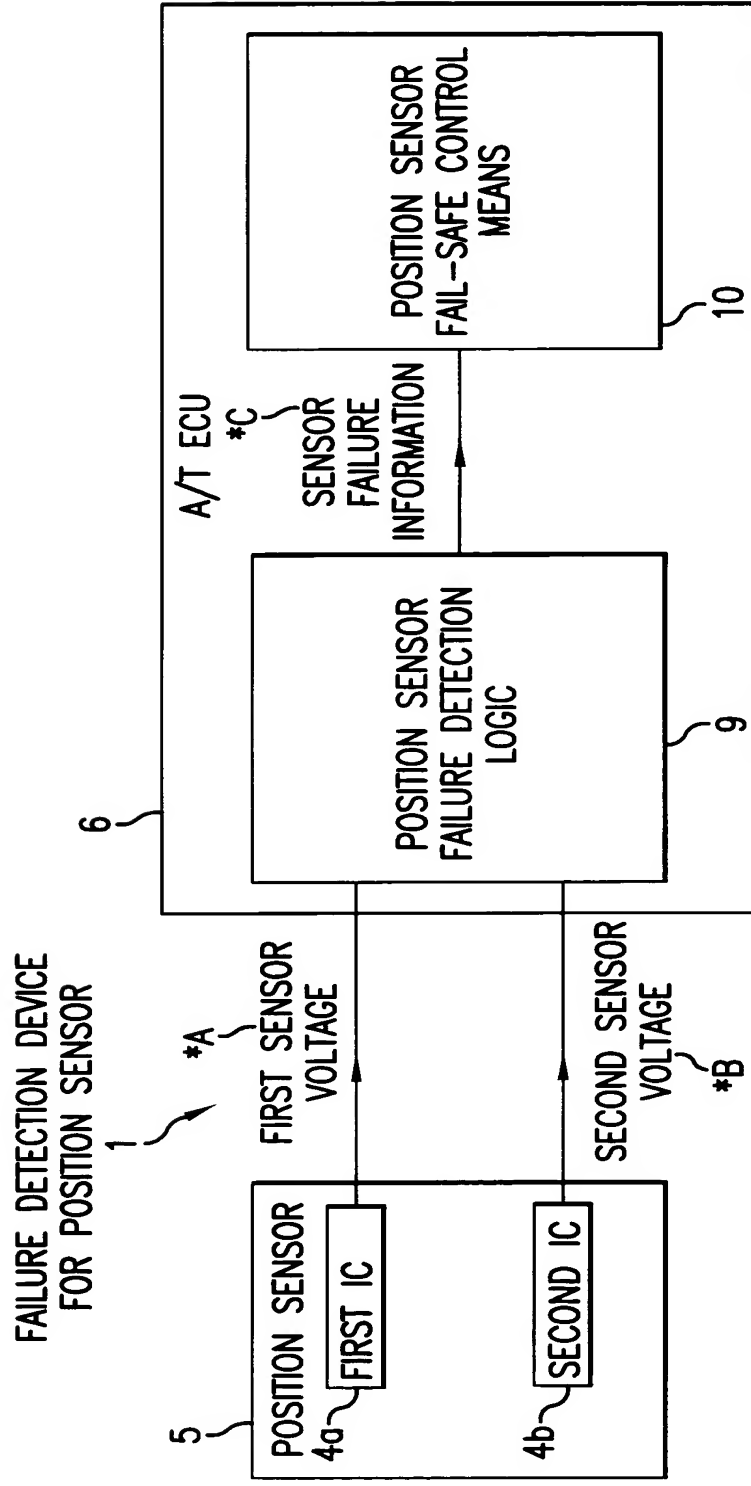


FIG.3

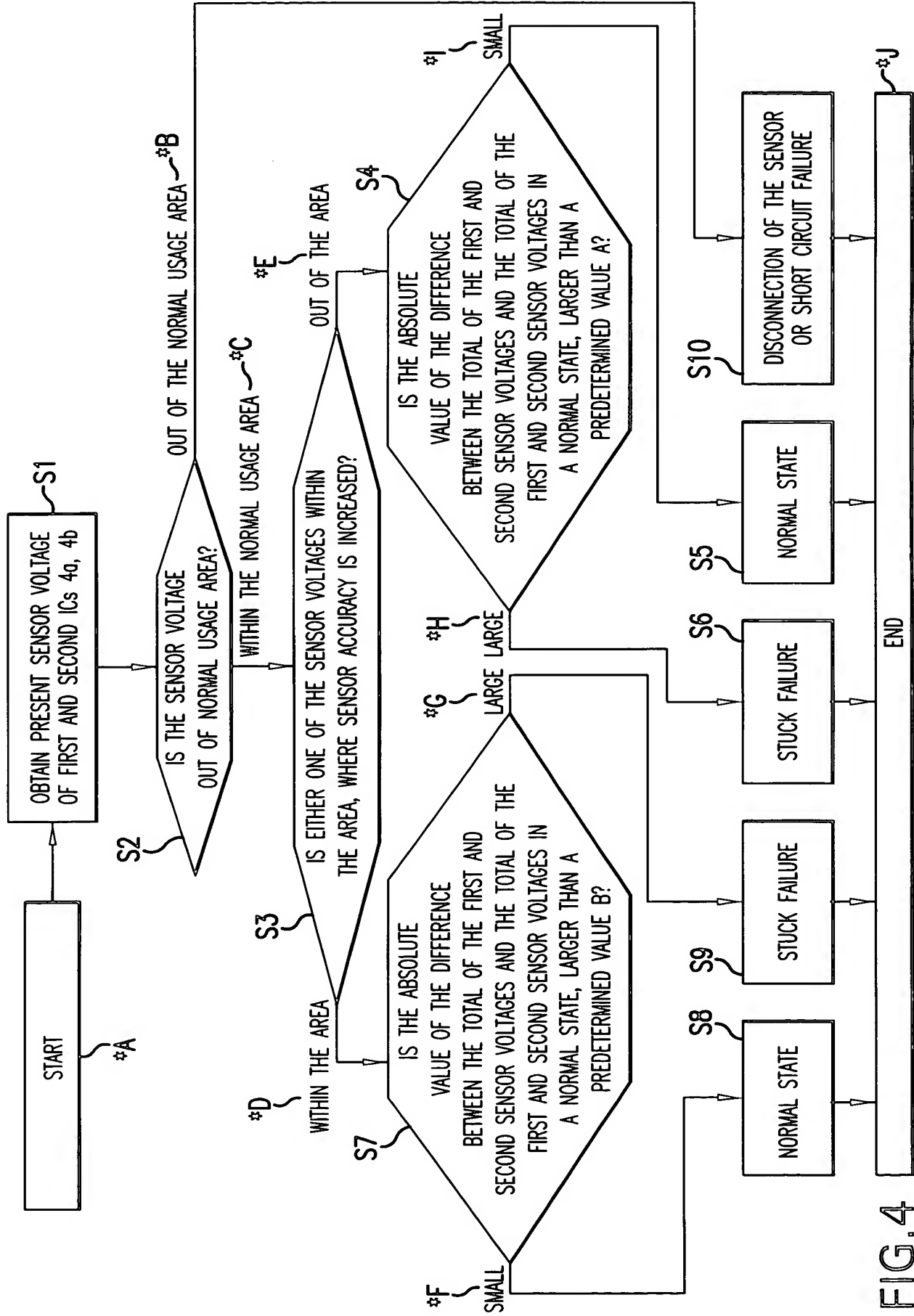


FIG. 4

*D~VOLTAGE STUCK FAILURE OF THE SECOND IC 4b IS GENERATED

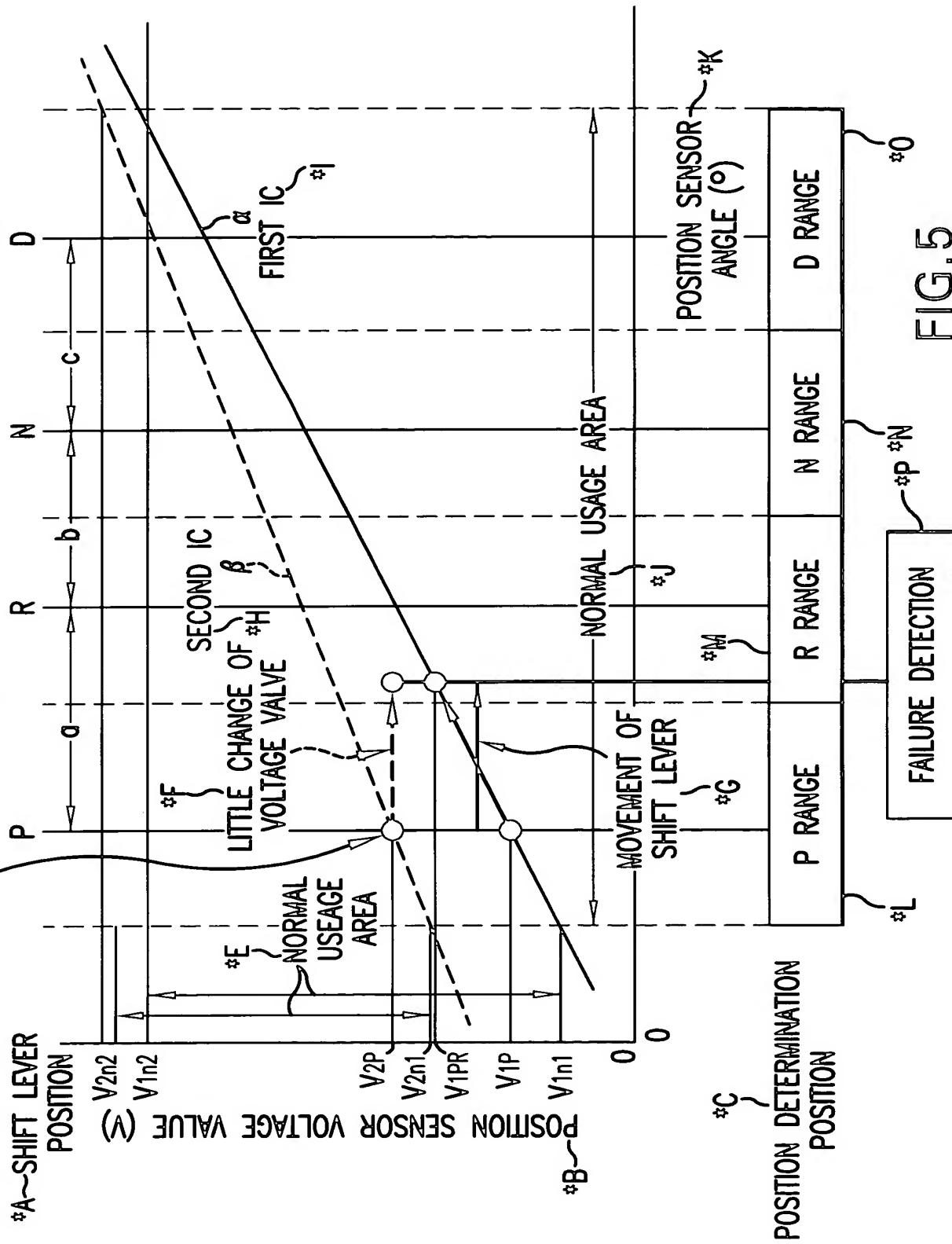


FIG.5